REMARKS

We are in receipt of the Office Action dated August 24, and the above Amendment and following remarks are made in light thereof.

Claims 1, 3, 15, 18, 21, 24, 27-34 and 42-49 are under consideration in the present application. In the Office Action of August 24, 2001, each of these claims stands rejected under 35 U.S.C. 103 as being unpatentable over Chang et al., U.S. Patent 5,893,740, in view of Ko et al., U.S. Patent 5,686,321, and/or Mikoshiba, JP 56-060061 A. This rejection was made "Final."

The present invention relates to a semiconductor device formed in a single semiconductor substrate, wherein an impurity is introduced from the < 110> axis, that is, from a diagonal direction in range of 45°±3° with respect to a surface of the single semiconductor substrate.

In the Office Action the Examiner notes that Mikoshiba teaches that the MOSFET can be formed with the wafer surface being parallel to the (100) crystal plane and with the channel being aligned to the <100> crystal direction for minimizing the adverse piezo effect.

However, Mikoshiba shows the source 3 and drain 4 being disposed in the <100> direction at 45 degrees with respect to the flat part 2 so that the channel direction is coincident with the <100> direction. On the other hand, the claimed invention recites introducing an impurity into the single semiconductor substrate along the <110> direction, which is an oblique direction of about 45° degrees with respect to the surface of the single crystal semiconductor substrate. Thus, damage in the impurity introducing step can be minimized because silicon has the smallest atom density on the {110} face (page 4, lines 11-13).

Mikoshiba does not teach reducing the damage in the impurity introducing step, but locating the source, drain and channel so as to minimize the piezo effect. In addition, while the

present invention recites introducing the impurity at about 45° degrees with respect to the surface of the substrate, the reference shows forming the source, drain and channel with respect to the flat part 2. Therefore, the reference does not disclose or suggest the claimed invention.

Chang teaches a large-angle-tilt implant to form an ion-implanted region 18 (col. 3, lines 49-54). However, the reference does not include an influence for the lattice of the single crystal semiconductor in the implant process. Thus, Chang's et al. device has the problem described in the Background of the Invention in the specification. That is, the damage to the crystal lattice can not be prevented. In addition, the impurity ion remains in where the channel is formed through the process of the injecting the impurity ions into the substrate (page 3, lines 13-14)

Although Chang et al. indicates the angle of the implant step can include an angle generator than about 30 degrees from a perpendicular from the gate electrode (col.2,lines 35-38), this range of the angle is not determined based on reviewing the influence on the crystal lattice.

As mentioned above, the object of determining locations of the source, drain and channel with the angle in Mikoshiba is different from that of introducing the impurity ion with the angle in the present invention. Chang et al. does not teach minimizing the damage in the implant step. Therefore, it is not obvious in the art that to realize the claimed invention by combining Mikoshiba and Chang et al.

Ko et al. discloses using ion implantation in which a punchthrough stop region 24 is formed (Fig. 1C, and col. 3, lines 27-31). However, the ion implantation is carried in a vertical direction with respect to the surface of the substrate. Further, the impurity ions are implanted through a gate oxide layer 24. Accordingly, the implantation process of Ko et al. is distinct from

the invention, and there is no motivation to combine the concentration of Ko et al. with the large/angle/tilt implant of Chang et al.

Accordingly, Applicant respectfully submits that the obviousness rejection is not supported by the combination with Chang et al., Ko et al. and Mikoshiba. Thus reconsideration and allowance is respectfully requested.

Respectfully submitted,

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In Re Application of)
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Akiharu MIYANAGA et al.)
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Serial No.: 09/241,695)
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Filed: February 2, 1999)
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For: Semiconductor Device And)
Process For Producing The Same)
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Art Unit: 2811)
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

wherein the second impurity is introduced with a diagonal direction in a range of 45°+3° with respect to a surface of the single crystal semiconductor substrate.

27. A device according to claim 1, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

28. A device according to claim 1, wherein the single crystal semiconductor substrate is a single silicon substrate.

29. A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region;

a pair of LDD regions, wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the second concentration of the impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the second impurity is introduced with a diagonal direction in a range of 45°+3° with respect to a surface of the single crystalline semiconductor substrate.

34. A device according to claim 29, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

42. A semiconductor device comprising at least a CMOS circuit including an n-channel MOSFET and a p-channel MOSFET each being formed in a single crystal semiconductor substrate,

said n-channel MOSFET comprising:

a first source region and a first drain region each comprising a first n-type impurity;

a first channel forming region being formed between the first source region and the first drain region;

a first impurity region including a first p-type impurity and being formed under the first channel forming region;

said p-channel MOSFET comprising:

a second source region and a second drain region each comprising a second p-type impurity;

a second channel forming region being formed between the second source region and the second drain region;

a second impurity region including a second n-type impurity and being formed under the second channel forming region,

wherein each of the first p-type and the second n-type impurities is introduced from a direction of the <110> axis with respect to the single crystal semiconductor substrate, so that each of the first p-type and the second n-type impurities is introduced from a perpendicular direction to a plan having the smallest atomic density of the single crystal semiconductor substrate,

wherein a concentration of the first p-type impurity in the first impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the first p-type impurity in the first channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein a concentration of the second n-type impurity in the second impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the second n-type impurity in the second channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein each of the first p-type and the second n-type impurities is introduced with a diagonal direction in a range of 45°+3° with respect to a surface of the single crystal semiconductor substrate.

48. (Amended) A device according to claim 42, wherein each of the first and second impurity regions is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.